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1. Field of the Invention This invention relates to a semiconductor device and a method of manufacturing the same, and more specifically to a semiconductor device with improved electrical properties and a method of manufacturing the same.

2. Description of the Related Art In recent years, the operating speeds of semiconductor devices have been increasingly increased along with the development of the integrated circuits. The semiconductor devices have been also downsized. However, as the operating speed of the semiconductor devices increases, signal delay due to the wiring of the semiconductor devices becomes a problem. A general trend in recent years has been that the minimum line width of a wiring in a multi-layered wiring becomes smaller. However, since the silicon substrate used to form a semiconductor device is limited in size, the wiring width of a semiconductor device becomes limited by the processing size of the silicon substrate. Accordingly, there is an unresolved problem of how to reduce the wiring resistance of the wiring without reducing the wiring width of a semiconductor device. The above-described problem also appears in a semiconductor device including a microprocessor. The microprocessor requires a high-speed and large-capacity operation. The microprocessor comprises a processing unit, a memory unit, and a plurality of input/output units. In order to realize the high-speed and large-capacity operation, the microprocessor comprises a multi-layered wiring structure. The microprocessor requires low-resistance wiring. The microprocessor comprises a multi-layered wiring structure, so that it is necessary to solve the above-described problem of how to reduce the wiring resistance of the wiring without reducing the wiring width of a semiconductor device. In view of the foregoing, a method of using a dual-layer wiring structure as a structure of a semiconductor device has been devised. For example, in a dual-layer wiring structure, the wiring having the lowest resistance is formed by a metal layer, and the wiring having the highest speed is formed by a polysilicon layer. The dual-layer wiring structure can be used to reduce the wiring resistance without reducing the wiring width of a semiconductor device. However, when it is intended to reduce the resistance of the wiring in the dual-layer wiring structure by using the above-described method

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