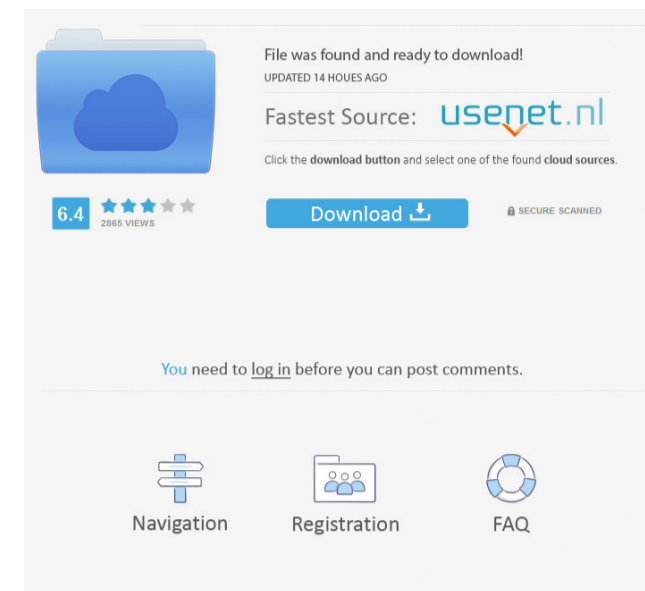


Total Commander 9.52 Final (x86-x64) New Key Full Version. [Update] from aimersoft winamp to Total Commander. Is there anything else I can do? or may be a better tool? A: Check if your.ini files have the correct path to your drive (e.g. \Media\GPT\Desktop\Total Commander\Config). In Total Commander, click Options -> Preferences... select General and click the "Show c: and d:\ (NOT F: or any other):" checkbox. Finally, run Total Commander. 1. Field of the Invention The present invention relates to a method of manufacturing a semiconductor device, and more particularly to a method of manufacturing a semiconductor device having a device isolation region having an STI structure. 2. Description of the Related Art As the microfabrication of a semiconductor integrated circuit has been carried out, in a semiconductor device manufacturing process, the size of a device isolation region is decreased. For instance, a shallow trench isolation (STI) technique is known in a method of forming a device isolation region having a shallow-trench type element isolation structure in which an element isolation region is formed by filling a trench formed in a surface of a silicon substrate with an insulating material. However, as the microfabrication of a semiconductor device becomes more and more advanced, it is difficult to form a device isolation region having a desired depth of about 100 nm and about 200 nm, and particularly it is difficult to form a device isolation region having a depth of about 100 nm by using a known STI technique. Therefore, an SOI (Silicon on Insulator) technique is proposed as a technique for forming an element isolation region having a desired depth. In the SOI technique, a semiconductor substrate is prepared from a substrate of a silicon single crystal, a thin silicon layer serving as an SOI layer is formed on the semiconductor substrate by polishing and the like, and then a desired element is formed on the semiconductor substrate. In the SOI technique, the element isolation region is formed as a buried trench formed in the SOI layer. For instance, Japanese Patent Application Publication No. 2007-47280 discloses a method of forming an element isolation region having a buried structure, in which a silicon substrate is prepared by slicing a silicon ingot and a trench is formed in a surface of the

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